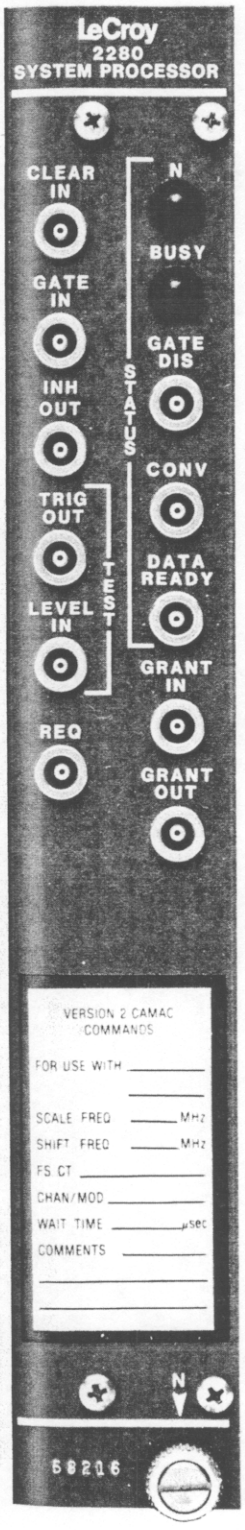
SPECIFICATIONS
CAMAC Model 2280
SYSTEM PROCESSOR



FRONT PANEL INPUTS
(LEMO TYPE CONNECTORS)

Gate: 50 Ω impedance. – 600 mV or greater enables. Distributed to ADC modules via ASB. Gates received after start of conversion are locked out. Use of gate disabled output recommended to avoid partial gating during enabling or fast clearing. 50 nsec minimum width.

Clear: Common to all ADC's. 50 Ω impedance. – 600 mV or greater enables. 50 nsec minimum width. (See individual ADC specifications for settling time.) Distributed to ADC modules via the ASB.

Test Level: During the test cycle a signal proportional to the applied voltage (internal high impedance connection to +8 V) will be present at all ADC inputs about 20 nsec after gate opening. Distributed via ASB.

Grant In: Requires TTL clamp to ground (for Type A2 CAMAC controller).

FRONT PANEL LED's
(Internally stretched to 1 msec minimum)

N Light: Indicates when unit is being addressed.

Busy Light: Indicates when the Model 2280 has seized control of the CAMAC dataway.

FRONT PANEL OUTPUTS
(LEMO TYPE CONNECTORS)

Test Trigger: Provides NIM level signal of 1μsec duration to trigger external gate logic when processor receives F(25)•A(1)

Gate Disabled: Provides TTL clamp to ground whenever processor is not ready to receive a gate.

Conversion: Provides TTL clamp to ground from trailing edge of gate until end of conversion.

Data Ready: Provides TTL clamp to ground from end of conversion, if data was stored in memory, until last word is read or unit is cleared.

Request: Provides TTL clamp to ground (for Type A2 CAMAC controller).

Grant Out: Provides TTL clamp to ground (for Type A2 CAMAC controller).

SYSTEM OPERATION

Conversion (Scaling & Data Transfer): The System must first be enabled by an F(26)•A(4). This commands the processor to take control of the CAMAC crate, which then causes the CAMAC BUSY to be clamped, resets the ADC's, and permits acceptance of an external gate to the processor (which is transmitted to the ADC's via the ASB). After a "wait" time (to allow for a fast clear) the processor supplies the scaler clock train required by the ADC's followed by readout of each module. Data of groups of twelve ADC channels are simultaneously shifted out serially to the processor via dataway buses R13 - R24. The data are converted to parallel form, preprocessed (see Pedestal Subtraction and Data Compression), and stored in the data memory. When all data are processed, the processor is automatically disabled, the BUSY line is released, and a LAM is generated.

Pedestal Subtraction: The processor contains a 1024-word by 12-bit pedestal memory. This memory is loaded from the dataway by sequentially writing up to 1008 pedestal values using F(16)•A(0). If pedestal subtraction has been selected via coding of the F(16)•A(3) control word, incoming ADC data is automatically corrected before being loaded into the processor's memory.